C O M P O N E N T S

Zilog

The Measure of Performance

D A T A B O O K

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*New Document

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Part Number Index

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All 85XX components are compatible with processors other than Zilog's Z8001, Z8002, Z8003, and Z8004. For further information refer to the individual product specifications.

Military Product Cross Reference

Products Are Available in MIL-STD-883 Class B Flow Unless Otherwise Noted (†).

Device	Speed in MHz					Package		JAN	
	2.5	4.0	6.0	8.0	10.0	C(DIP) Pins	L(LCC) Pins	MIL-M-38510	Description
*Z8001		X				48	(@) 68	F	Z8000 SEG CPU
*Z8001A			X			48	(@) 68	F	Z8000 SEG CPU
*Z8001B					X	48	(@) 68	F	Z8000 SEG CPU
*Z8002		X				40	(†) 44	Q	Z8000 NON-SEG CPU
*Z8002A			X			40	(†) 44	Q	Z8000 NON-SEG CPU
*Z8002B					X	40	(†) 44	F	Z8000 NON-SEG CPU
*Z8010		X				(†) 48	(@) 68		Z8000 Z-MMU Z-BUS
*Z8010A			X			(†) 48	(@) 68		Z8000 Z-MMU Z-BUS
*Z8010B					X	(†) 48	(@) 68		Z8000 Z-MMU Z-BUS
Z8030		X				40	(†) 44	F	Z8000 Z-SCC Z-BUS
Z8030A			X			40	(†) 44	F	Z8000 Z-SCC Z-BUS
Z8530		X				40	(†) 44	F	Z8000 SCC Multi Bus
Z8530A			X			40	(†) 44	F	Z8000 SCC Multi Bus
Z8036		X				40	(†) 44	F	Z8000 Z-CIO Z-BUS
Z8036A			X			40	(†) 44	F	Z8000 Z-CIO Z-BUS
Z8536		X				40	(†) 44	F	Z8000 CIO Multi Bus
Z8536A			X			40	(†) 44	F	Z8000 CIO Multi Bus
Z8038		X				(@) 40	(@) 44	F	Z8000 Z-FIO Z-BUS
Z8038A			X			(@) 40	(@) 44	F	Z8000 Z-FIO Z-BUS
Z8581			X			(†) 18	(TBD) 44	F	Z8000 CGC
Z8581-10					X	(†) 18	(TBD) 44	F	Z8000 CGC
Z8400	X					40	(†) 44	Q	Z80 CPU
Z8400A		X				40	(†) 44	Q	Z80 CPU
Z8420	X					40	(†) 44		Z80 PIO
Z8420A		X				40	(†) 44		Z80 PIO
Z8430	X					28	(†) 44		Z80 CTC
Z8430A		X				28	(†) 44		Z80 CTC
Z8440	X					40			Z80 SIO/0
Z8440A		X				40			Z80 SIO/0
Z8441	X					40			Z80 SIO/1
Z8441A		X				40			Z80 SIO/1
Z8442	X					40			Z80 SIO/2
Z8442A		X				40			Z80 SIO/2
Z8444	X						(†) 44		Z80 SIO/0,1,2
Z8444A		X					(†) 44		Z80 SIO/0,1,2
Z8611				X		(†) 40	(TBD) 44		Z8 MCU
Z8671				X		(†) 40	(TBD) 44		Z8 MCU BASIC Debug
Z8681				X		(†) 40	(TBD) 44		Z8 ROMless

*Available in −55°C to +110°C temperature range.

@ Future Package, contact your local sales representative for current availability.
† Device/Package currently available in military temperature range only. Contact your local sales representative for current Class B flow availability.
Q JAN qualified/dual-in-line package only.
F Future proposed JAN product/dual-in-line package only.
TBD To be determined.

Z8400
Z80® CPU Central Processing Unit

Zilog

Product Specification

April 1985

FEATURES

- The instruction set contains 158 instructions. The 78 instructions of the 8080A are included as a subset; 8080A software compatibility is maintained.
- Eight MHz, 6 MHz, 4 MHz, and 2.5 MHz clocks for the Z80H, Z80B, Z80A, and Z80 CPU result in rapid instruction execution with consequent high data throughput.
- The extensive instruction set includes string, bit, byte, and word operations. Block searches and block transfers, together with indexed and relative addressing, result in the most powerful data handling capabilities in the microcomputer industry.
- The Z80 microprocessors and associated family of peripheral controllers are linked by a vectored interrupt system. This system may be daisy-chained to allow implementation of a priority interrupt scheme. Little, if any, additional logic is required for daisy-chaining.
- Duplicate sets of both general-purpose and flag registers are provided, easing the design and operation of system software through single-context switching, background-foreground programming, and single-level interrupt processing. In addition, two 16-bit index registers facilitate program processing of tables and arrays.
- There are three modes of high speed interrupt processing: 8080 similar, non-Z80 peripheral device, and Z80 Family peripheral with or without daisy chain.
- On-chip dynamic memory refresh counter.

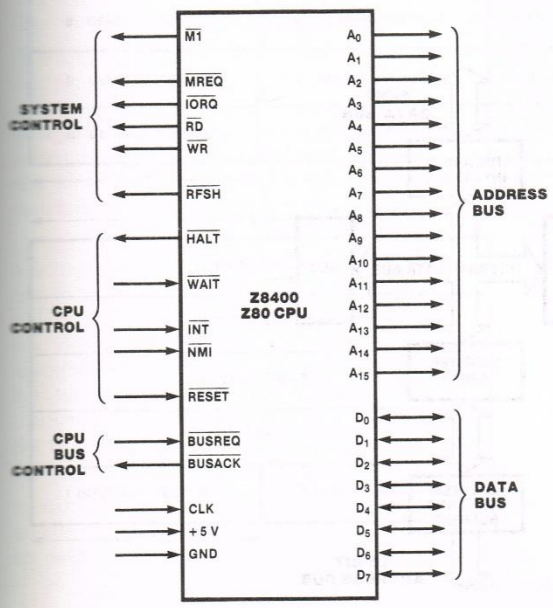

Figure 1. Pin Functions

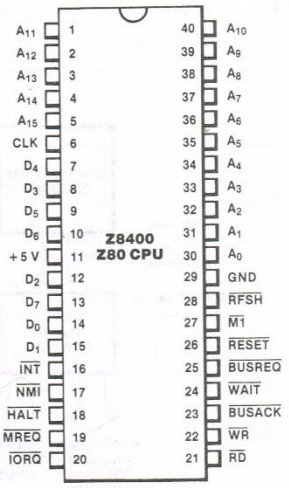

Figure 2a. 40-Pin Dual-In-Line Package (DIP) Pin Assignments

Z8® Z8601
Z8® Z8603

Product Specification

Zilog

Z8601 Single-Chip Microcomputer with 2K ROM
Z8603 Prototyping Device with EPROM Interface

April 1985

Features

- Complete microcomputer, 2K bytes of ROM, 128 bytes of RAM, 32 I/O lines, and up to 62K bytes addressable external space each for program and data memory.
- 144-byte register file, including 124 general-purpose registers, four I/O port registers, and 16 status and control registers.
- Average instruction execution time of 1.5 μs, maximum of 3 μs.
- Vectored, priority interrupts for I/O, counter/timers, and UART.
- Full-duplex UART and two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler.
- Register Pointer so that short, fast instructions can access any of nine working register groups in 1 μs.
- On-chip oscillator that accepts crystal or external clock drive.
- Single +5 V power supply—all pins TTL-compatible.

General Description

The Z8601 microcomputer introduces a new level of sophistication to single-chip architecture. Compared to earlier single-chip microcomputers, the Z8601 offers faster execution; more efficient use of memory; more sophisticated interrupt, input/output and bit-manipulation capabilities; and easier system expansion.

Under program control, the Z8601 can be tailored to the needs of its user. It can be configured as a stand-alone microcomputer with 2K bytes of internal ROM, a traditional microprocessor that manages up to 124K bytes of external memory, or a parallel-processing element in a system with other processors and peripheral controllers linked by the Z-BUS. In all configurations, a large number of pins remain available for I/O.

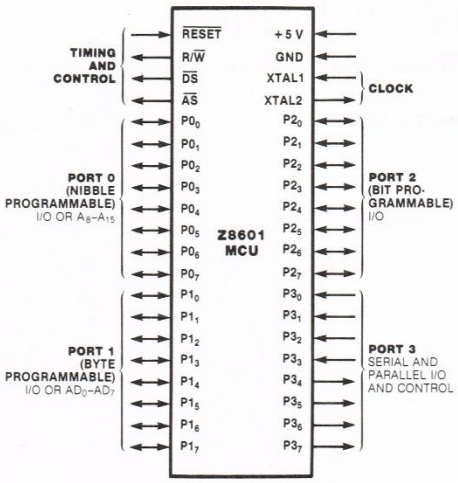

Figure 1. Pin Functions

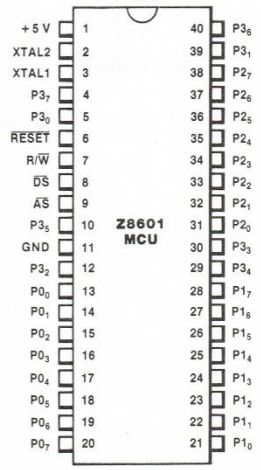

Figure 2a. 40-pin Dual-In-Line Package (DIP), Pin Assignments

Super-8 Family of Microcomputers

Zilog

NEW 1985

Preliminary Product Specification

April 1985

FEATURES

- Improved Z8 instruction set includes multiply and divide instructions, Boolean and BCD operations.
- Additional instructions support threaded-code languages, such as "Forth."
- 325 byte registers, including 272 general-purpose registers, and 53 mode and control registers.
- From 0 to 16 Kbytes of on-chip ROM with external addressing up to 128K bytes.
- Two register pointers allow use of short and fast instructions to access register groups within 600 ns.
- Direct Memory Access controller (DMA).
- Two 16-bit counter/timers.
- Up to 40 bit-programmable I/O lines, with 2 handshake channels.
- Interrupt structure supports:
  - 37 interrupt sources
  - 16 interrupt vectors
  - 8 interrupt levels
  - Servicing in 600 ns. (1 level only)
- Full-duplex UART with special features.
- Optional additional synchronous/asynchronous multi-protocol serial channel (available 1986).
- Optional low-power standby capability permits saving of register contents.
- Multiple versions permit design flexibility, efficient product development, and cost-effective production.
- On-chip oscillator.
- 20 MHz clock.
- Choice of 40- or 48-pin packages.

GENERAL DESCRIPTION

The Zilog Super-8 family of single-chip microcomputers offers a comprehensive selection of MCUs for development and production. They can be used as I/O- or memory-intensive computers, or they can be configured to address external memory while still supporting many I/O lines.

The Super-8 is available in several different packages and configurations. They offer varying amounts of ROM and I/O ports, and a choice of addressing capabilities. They all feature a full-duplex universal asynchronous receiver/transmitter (UART) with on-chip baud rate generator, two programmable counter/timers, a direct memory access (DMA) controller, and an on-chip oscillator.

The Super-8 is available with 4, 8, or 16 Kbytes of internal ROM, in 40- or 48-pin packages, and with four or five I/O ports. A group of similarly packaged protopack Super-8s is available with a "piggy-back" EPROM interface. ROMless versions are also available in 40- and 48-pin packages. A special development chip, designed for emulation, is also available.

Z800™ MPU Family

Zilog

Preliminary Product Specification

September 1983

FEATURES

- Enhanced Z80® instruction set that maintains object-code compatibility with Z80 microprocessor.
- On-chip paged Memory Management Unit (MMU).
- Large memory address space: 512K byte and 16M byte versions.
- On-chip, high-speed local or cache memory.
- High performance 16-bit Z-BUS interface or 8-bit Z80-compatible bus interface.
- Four on-chip 16-bit counter/timers.
- Four on-chip DMA channels.
- On-chip full duplex UART.
- 10-25 MHz CPU processor clock.

GENERAL DESCRIPTION

Zilog's new Z800 family of 8- and 16-bit microprocessors features high-performance microprocessors designed to give the end-user a powerful and cost effective solution to application requirements. The family consists of the Z80-Bus microprocessors that are packaged in 40- and 64-pin dual in-line packages, and 16-bit Z-BUS microprocessors in 40- and 64-pin packages. The Z800 family incorporates advanced architectural features that allow fast and efficient throughput and increased memory addressing while maintaining Z80 object code compatibility. Z800 microprocessors offer both a continuing growth path for present Z80-based designs and a high-performance microprocessor for future designs.

Central to the Z800 microprocessors is an enhanced version of the Z80 Central Processing Unit (CPU). To assure system integrity, the Z800 microprocessors can operate in either user or system mode, allowing protection of system resources from user tasks and programs. System mode operation is supported by the addition of a system Stack Pointer to the working register set. The IX and IY registers have been modified so that in addition to their regular function as index registers, each register can be accessed as a 16-bit general purpose register or as two single-byte registers.

The Z80 CPU instruction set has been retained, meaning that the Z800 microprocessors are completely binary-code compatible with present Z80 code. The basic addressing modes of the Z80 microprocessor have been augmented with the addition of Indexed mode with full 16-bit displacement, Program Counter Relative with 16-bit displacement, Stack Pointer Relative with 16-bit displacement, and Base Index mode. The new addressing modes are incorporated into many of the old Z80 CPU instructions, resulting in greater flexibility and power. Some additions to the instruction set include 8-and 16-bit signed and unsigned multiply and divide, 8-and 16-bit sign extension, and a test and set instruction to support multiprocessing. The 16-bit instructions have been expanded to include 16-bit compare, memory increment, memory decrement, negate, add, and subtract, in addition to the previously mentioned multiply and divide.

A requirement of many of today's microprocessor-based system designs is to increase the memory address space beyond the 64K byte range of typical 8-bit microprocessors. The Z800 microprocessors have an on-chip Memory Management Unit (MMU) that enables the microprocessors to address either 512K bytes or 16M bytes, depending on the device package. In addition to enabling the address space to be expanded, the MMU performs other memory management functions previously handled by dedicated off-chip memory management devices.

I/O address space has been expanded by the addition of an I/O Page register used to select pages of I/O addresses. The 8-bit I/O Page register can select one of

256 possible pages of I/O addresses to be active at one time, allowing a total of 64K I/O addresses to be accessed.

There are 256 bytes of on-chip memory present on all members of the Z800 family. This memory can be configured as a high-speed cache or as a fixed address local memory. When configured as a cache, the memory can be programmed to be instruction only, data only, or both data and instruction. The cache memory allows programs to run significantly faster by reducing the number of external bus accesses. Operation and update of the cache is performed automatically and is completely transparent to the user. When used as a local memory, the addresses are programmable, allowing "RAMless" systems to be used.

Many features that have traditionally been handled by external peripheral devices have been incorporated in the design of the Z800 microprocessors. The "on-chip peripherals" reduce system chip count and reduce interconnection on the external bus. All members of the Z800 family contain an on-chip clock oscillator. Also present is a refresh controller that provides 10-bit refresh addresses for dynamic memories.

The 64-pin versions of the Z800 MPU contain additional on-chip peripherals to provide system design flexibility. To support high-bandwidth data transmission, four Direct Memory Access (DMA) channels are incorporated on-chip. Each DMA channel operates using full 24-bit source and destination addresses with a 16-bit count. The channels can be programmed to operate in single transaction, burst, or continuous mode. System event counting and timing requirements are met with the help of the four 16-bit counter/timers. The counter/timer functions can be externally controlled with gate and trigger inputs, and can be programmed as retriggerable or nonretriggerable. Also, a full duplex UART, capable of handling a variety of data and character formats, is present to facilitate asynchronous serial communication.

Regardless of whether the 8- or 16-bit bus is used, all members of the Z800 family feature programmable bus timing, allowing the user to tailor timing to the individual system. Upon reset the Z800 microprocessors can be programmed to have system timing that is one-fourth, one-half, or equal to the speed of the CPU, with one-half being the default. In addition to clock scaling, programmable wait states can be inserted during various bus transactions. Without the use of external hardware, one to three wait states can be inserted into memory, I/O, and interrupt acknowledge transactions. Furthermore, separate memory wait states can be specified for upper and lower memory areas, facilitating the use of different speeds of ROMs and RAMs in the same system.

An additional feature of the 16-bit bus interface is the ability to support "nibble-mode" dynamic RAMs. Using this feature (known as burst mode), the bus bandwidth of memory read transactions is essentially doubled. Burst mode transactions have the further benefit of allowing the cache to operate more efficiently by guaranteeing a high probability that the contents of the accessed memory will be present in the cache.

The Z800 family supports Zilog's Extended Processor Architecture (EPA) in a number of ways. All members are capable of trapping Extended Processor Unit (EPU) instructions in order to perform software emulation of the EPU. The Z8216 directly interfaces with an EPU such as the Z8070 Floating Point Unit and operates in a manner that is completely transparent to the user and the program. The other members of the Z800 family can interface easily with EPUs with the aid of support software.

The pin functions of four versions of the Z800 MPU, Z8108, Z8208, Z8116, and Z8216, are shown in Figures 1-4, respectively. A block diagram of the Z800 MPU is shown in Figure 5.

Z800 CPU

User and System Modes of Operation

The Z800 CPU can operate in either user or system mode. In user mode, some instructions cannot be executed and some registers of the CPU are inaccessible. In general, this mode of operation is intended for use by application programs. In system mode, all of the instructions can be executed and all of the CPU registers can be accessed. This mode is intended for use with programs that perform operating system functions. This separation of CPU resources promotes the integrity of the system, since programs operating in user mode cannot access those aspects of the CPU that deal with system interface events.

To further support the dual user/system mode, there are two copies of the Stack Pointer—one for the user stack and another for the system stack. These two stacks facilitate the task switching involved when interrupts or traps occur. To ensure that the user stack is free of system information, the information saved on the occurrence of interrupts or traps is always pushed onto the system stack before the new program status is loaded.

Z8001/2 Z8000® CPU
Central Processing Unit

Zilog

Product Specification

April 1985

FEATURES

- Regular, easy-to-use architecture
- Instruction set more powerful than many minicomputers
- Directly addresses 8 Mbytes
- Eight user-selectable addressing modes
- Seven data types that range from bits to 32-bit long words and byte and word strings
- System and Normal operating modes
- Separate code, data, and stack spaces
- Sophisticated interrupt structure
- Resource-shaping capabilities for multiprocessing systems
- Multi-programming support
- Compiler support
- Memory management and protection provided by Z8010 Memory Management Unit
- 32-bit operations, including signed multiply and divide
- Z-BUS compatible
- 4, 6, and 10 MHz clock rate

GENERAL DESCRIPTION

The Z8000 is an advanced high-end 16-bit microprocessor that spans a wide variety of applications ranging from simple stand-alone computers to complex parallel-processing systems. Essentially a monolithic minicomputer central processing unit, the Z8000 CPU is characterized by an instruction set more powerful than many minicomputers; abundant resources in registers, data types, addressing modes and addressing range, and a regular architecture that enhances throughput by avoiding critical bottlenecks such as implied or dedicated registers.

CPU resources include sixteen 16-bit general-purpose registers, seven data types that range from bits to 32-bit long words and byte and word strings, and eight user-selectable addressing modes. The 110 distinct instruction types can be combined with the various data types and addressing modes to form a powerful set of 414 instructions. Moreover, the instruction set is regular; most instructions can use any of the five main addressing modes and can operate on byte, word, and long-word data types.

The CPU can operate in either the system or normal mode. The distinction between these two modes permits privileged operations, thereby improving operating system organization and implementation. Multiprogramming is supported by the "atomic" Test and Set instruction; multiprocessing by a combination of instruction and

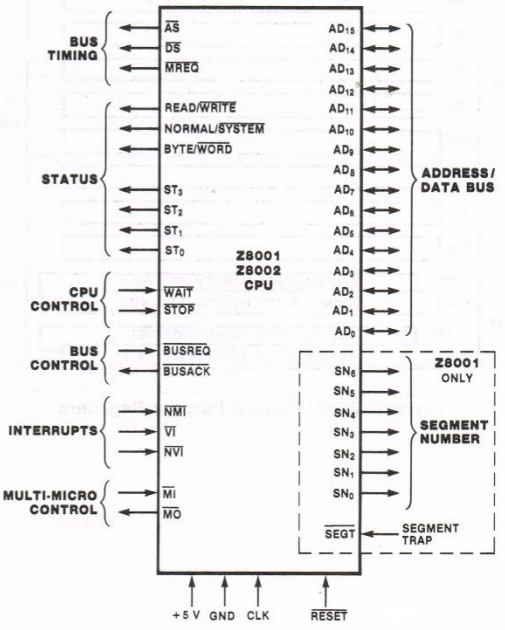

Figure 1. Z8000 CPU Pin Functions

Z80,000™ CPU

Zilog

Preliminary Product Specification

April 1985

FEATURES

- Full 32-bit architecture and implementation
- 4G (billion) bytes of directly addressable memory
- Linear or segmented address space
- Virtual memory management integrated with CPU
- On-chip cache memory
- General-purpose register file with sixteen 32-bit registers
- Nine general addressing modes
- Numerous data types include bit, bit field, logical value, signed integer, and string
- Extended Processing Architecture supports floating-point operations
- Regular use of operations, addressing modes, and data types in instruction set
- System and normal modes of operation with separate stacks
- Sophisticated interrupt and trap handling
- Software is a binary-compatible extension of Z8000™ software
- Hardware is compatible with other Z-BUS™ components
- Mainframe performance

GENERAL DESCRIPTION

The Z80,000 CPU is an advanced, high-end 32-bit microprocessor that integrates the architecture of a mainframe computer into a single chip. While maintaining full compatibility with Z8000 family software and hardware, the Z80,000 CPU offers greater power and flexibility in both its architecture and interface capability. Operating systems and compilers are easily developed in the Z80,000 CPU's high-quality environment, and the hardware interface provides for connection to a wide variety of system configurations.

Addresses in the Z80,000 CPU are 32 bits. This allows direct addressing of 4G bytes in each of four address spaces: system-mode data, system-mode instruction, normal-mode data, and normal-mode instruction. The CPU supports three modes of address representation. The 16-bit compact addresses are compatible with Z8000 nonsegmented mode. The 32-bit segmented addresses include both 16-bit offset, which is compatible with Z8000 segmented mode, and 24-bit offset. In addition a full 32-bit linear address space is provided.

The CPU features a general-purpose register file with sixteen 32-bit registers and nine operand addressing modes. The various addressing modes allow encoding choices for compact representation or for full 32-bit addressing. The instruction set can operate on bit, bit field, logical value, signed integer, unsigned integer, address, string, stack, and packed decimal byte data types. Logical and arithmetic instructions operate on bytes (8 bits), words (16 bits) and longwords (32 bits). The Extended Processing Architecture (EPA) supports floating-point operations. In addition, the instruction set is highly regular in combining operations, data types, and addressing modes. High-level language compilation is supported with instructions for procedure linkage, array index calculation, and bounds checking. Other instructions provide operating system functions such as system call and control of memory management.

There are two main operating modes, system and normal, supported by separate stacks. User programs operate in normal mode, while sensitive operating